

PH3230S

N-channel TrenchMOS™ logic level FET

Rev. 03 — 02 March 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level compatible
- High density mounting
- Low gate charge
- Very low on-state resistance.

1.3 Applications

- DC-to-DC converters
- Notebook computers
- Switched-mode power supplies
- Computer motherboards.

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $I_D \leq 100$ A
- $P_{tot} \leq 62.5$ W
- $R_{DSon} \leq 3.2$ mΩ.

2. Pinning information

Table 1: Pinning - SOT669 (LFAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view <small>MBL286</small></p> <p>SOT669 (LFAK)</p>	<p><small>MBB076</small></p>
4	gate (g)		
mb	drain (d)		



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3. Ordering information

Table 2: Ordering information

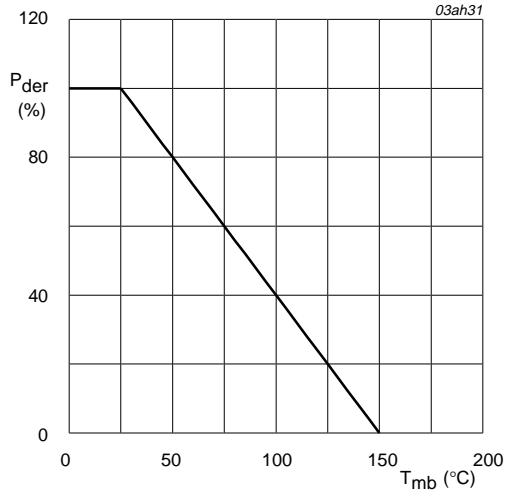
Type number	Package		Version
	Name	Description	
PH3230S	LFPAK	Plastic single-ended surface mounted package, 4 leads	SOT669

4. Limiting values

Table 3: Limiting values

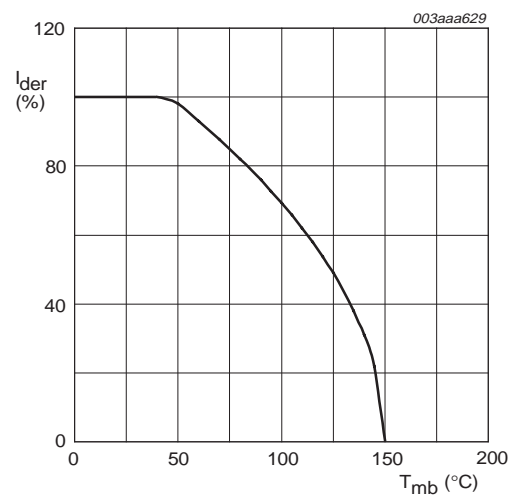
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2 and 3	-	100	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2	-	63	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	300	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	156	A
Avalanche ruggedness					
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	$T_j = 25\text{ °C}; R_{GS} \geq 50\text{ }\Omega; I_{DS(AL)R} = 5\text{ A};$ $V_{DD} = 15\text{ V};$ duty < 0.1%	-	2.5	mJ
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 50\text{ A};$ $V_{DD} \leq 15\text{ V}; R_{GS} = 50\text{ }\Omega; V_{GS} = 10\text{ V};$ starting $T_j = 25\text{ °C}$	-	250	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

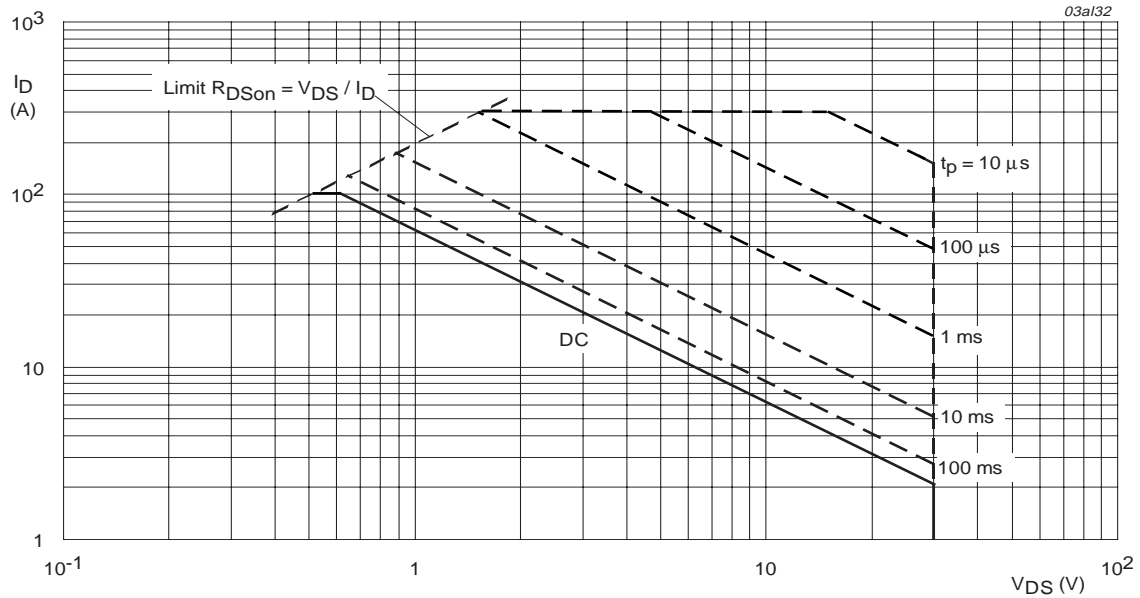
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$V_{GS} \geq 10 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance

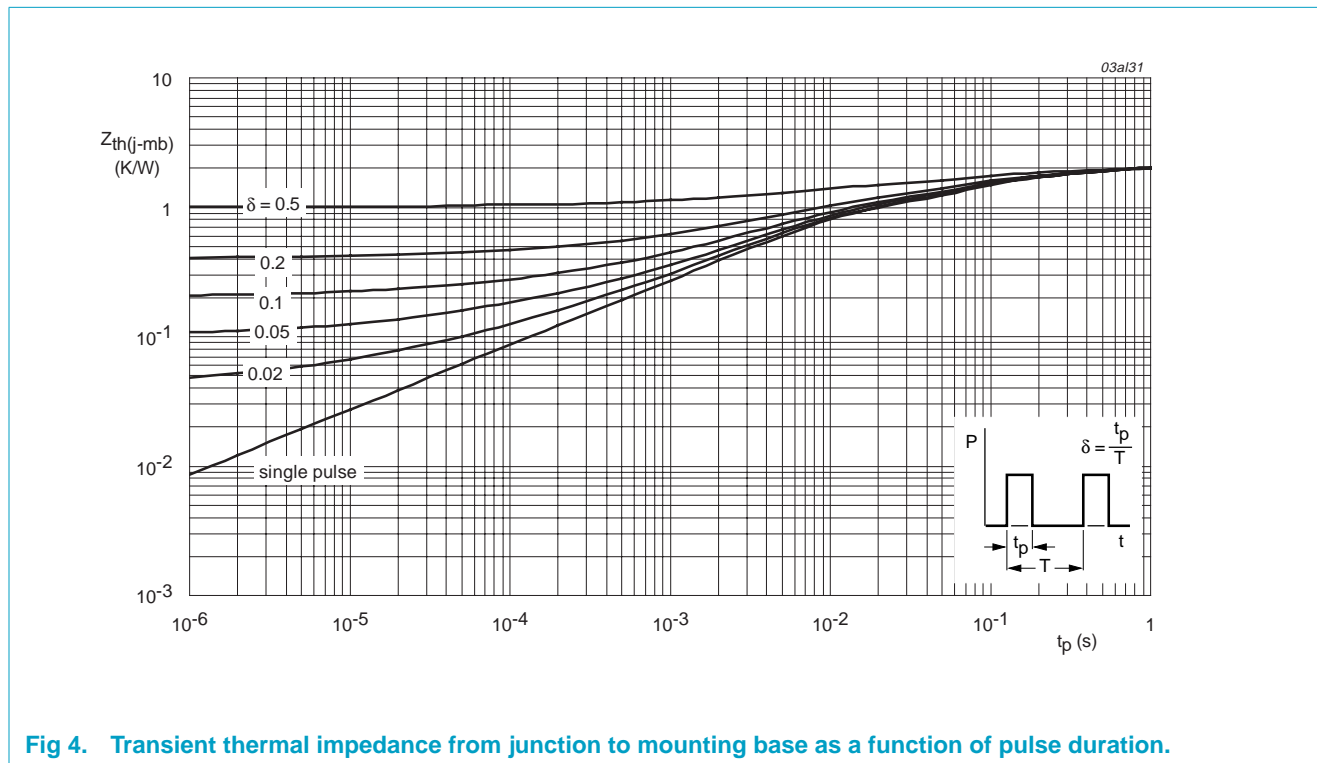


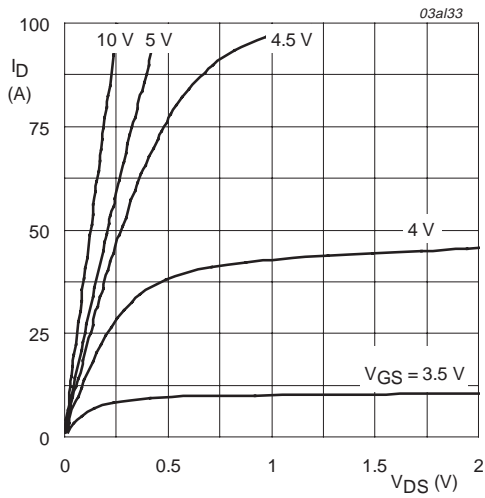
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

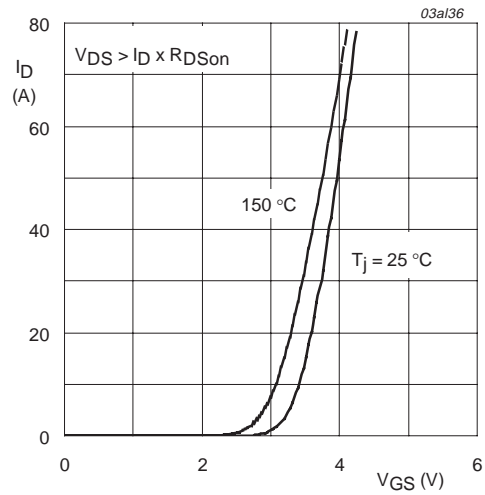
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ mA}$; $V_{GS} = 0\text{ V}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9	1	2	3	V
I_{DSS}	drain-source leakage current	$V_{DS} = 30\text{ V}$; $V_{GS} = 0\text{ V}$	-	-	1	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; Figure 7 and 8	-	2.7	3.2	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; Figure 8	-	5.0	6.5	m Ω
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 25\text{ A}$; Figure 11	39	75	-	S
$Q_{g(tot)}$	total gate charge	$I_D = 50\text{ A}$; $V_{DD} = 10\text{ V}$; $V_{GS} = 5\text{ V}$; Figure 14	-	42	-	nC
Q_{gs}	gate-source charge		-	21	-	nC
Q_{gd}	gate-drain (Miller) charge		-	13	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 10\text{ V}$; $f = 1\text{ MHz}$; Figure 12	-	4100	-	pF
C_{oss}	output capacitance		-	1150	-	pF
C_{rss}	reverse transfer capacitance		-	750	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\text{ V}$; $I_D = 25\text{ A}$; $V_{GS} = 10\text{ V}$; $R_G = 4.7\text{ }\Omega$	-	14	-	ns
t_r	rise time		-	37	-	ns
$t_{d(off)}$	turn-off delay time		-	85	-	ns
t_f	fall time		-	37	-	ns
Source-drain (reverse) diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 13	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -50\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$	-	46	-	ns



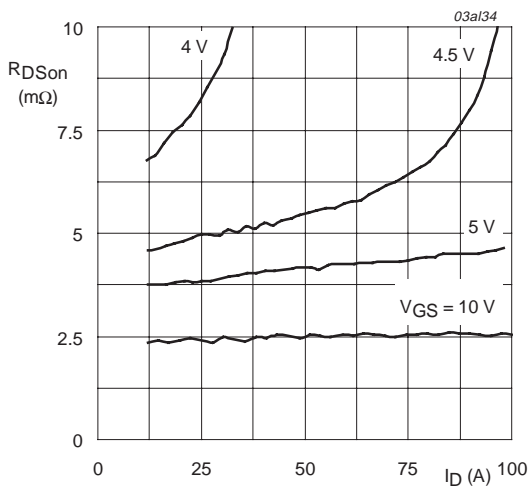
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



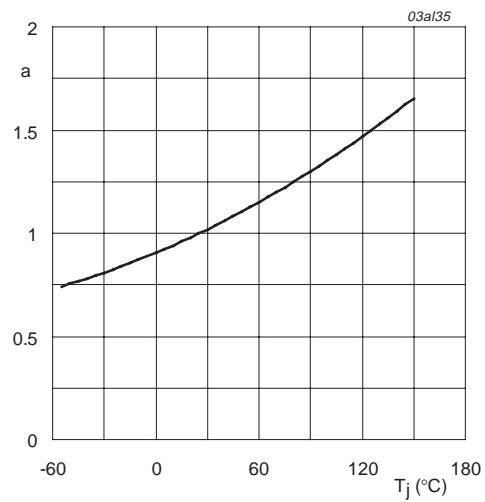
$T_j = 25\text{ °C}$ and 150 °C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



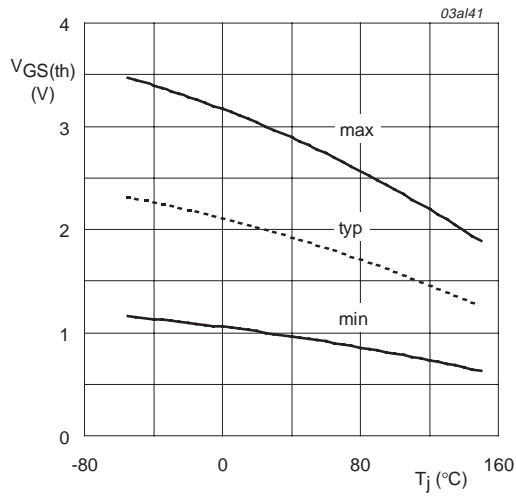
$T_j = 25\text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



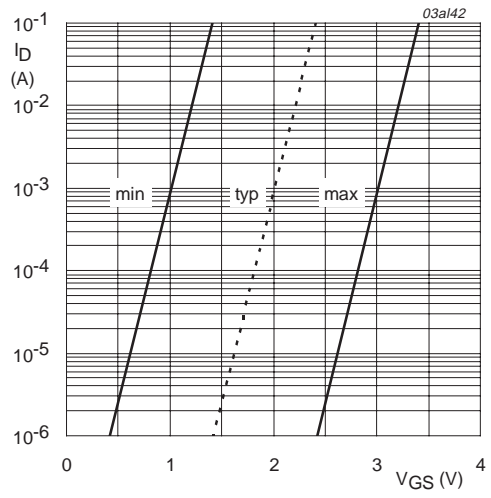
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



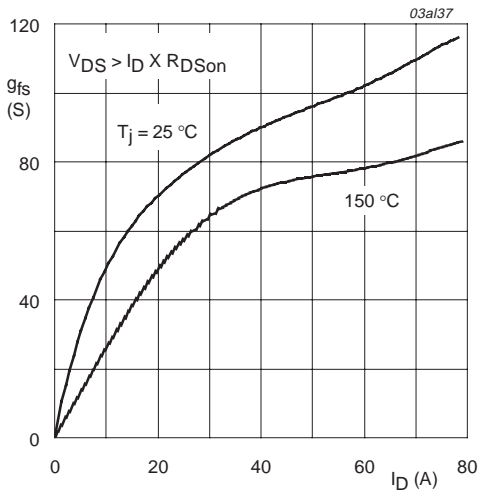
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



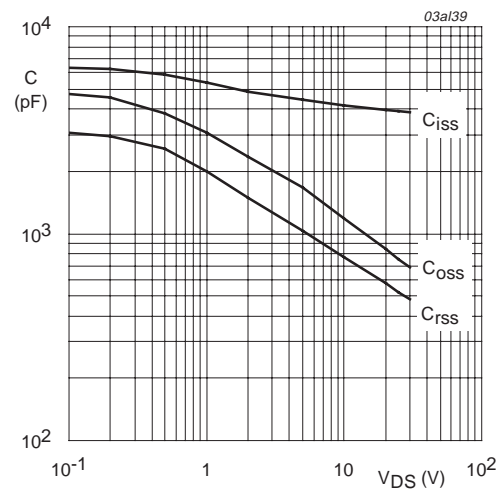
$T_j = 25 \text{ °C}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



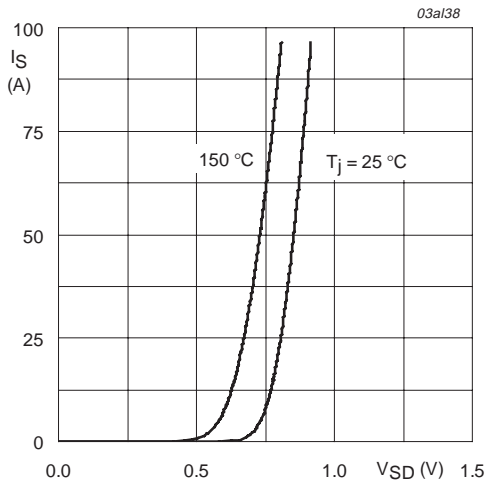
$T_j = 25 \text{ °C and } 150 \text{ °C}; V_{DS} > I_D \times R_{DSon}$

Fig 11. Forward transconductance as a function of drain current; typical values.



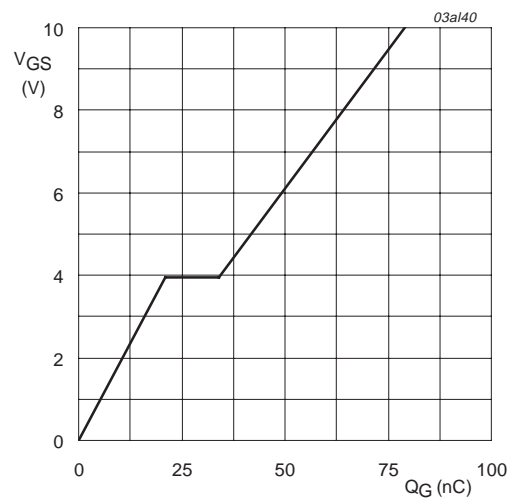
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$; $I_D = 50\text{ A}$; $V_{DD} = 10\text{ V}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic single-ended surface mounted package (Philips version LFAK); 4 leads

SOT669

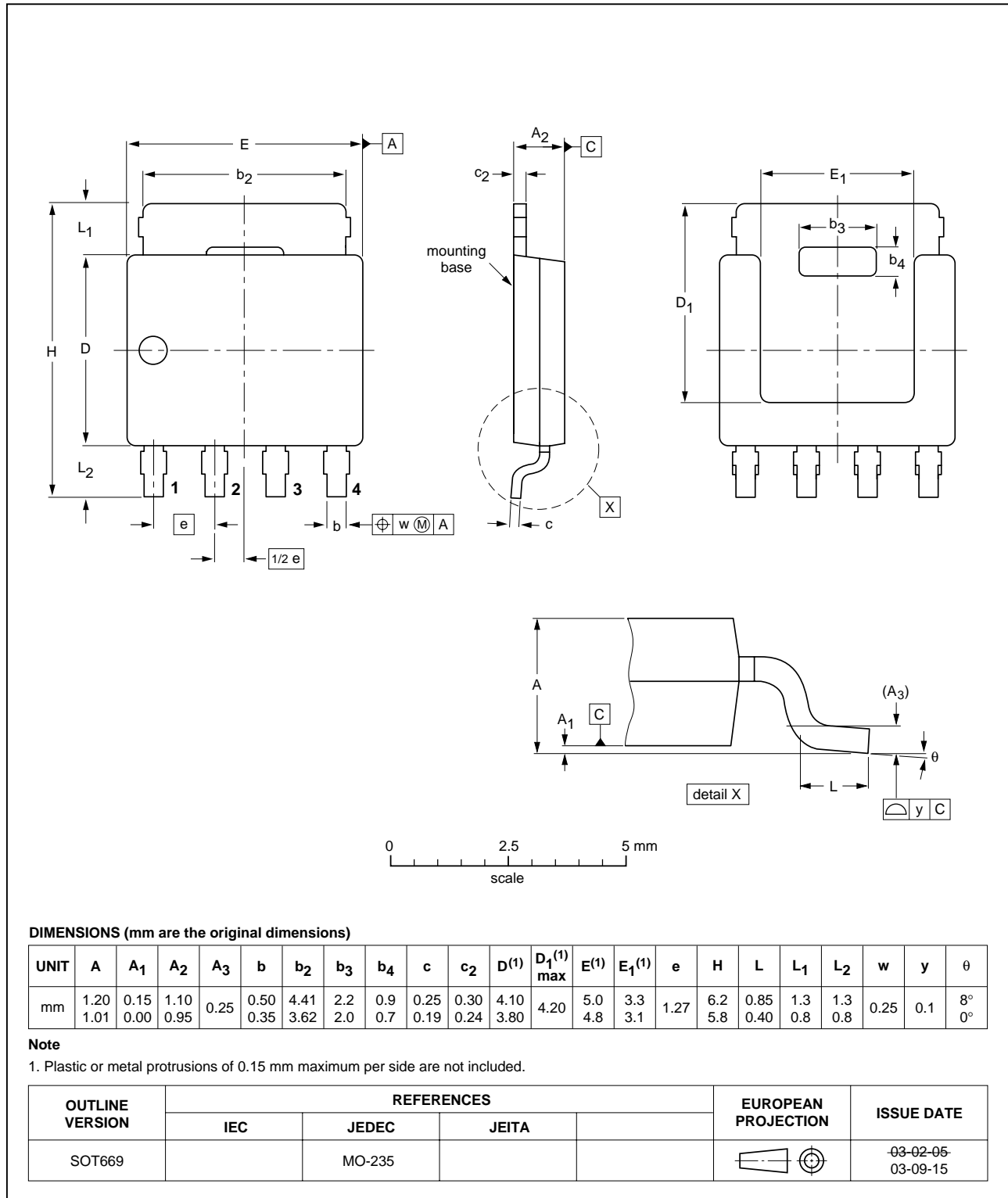


Fig 15. SOT669 (LFAK).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	20040302	-	Product data (9397 750 12756) Modifications: <ul style="list-style-type: none"> • I_D data corrected in Section 1.4 “Quick reference data” • g_{fs} typical value modified Table 5 “Characteristics” • V_{SD} condition and typical values modified Table 5 “Characteristics” • t_{rr} condition modified Table 5 “Characteristics” • t_r and t_f data corrected in Table 5 “Characteristics” • I_S data added in Table 3 “Limiting values” • I_{SM}, I_D and I_{DM} data corrected in Table 3 “Limiting values” • Correction to Figure 2 and Figure 3 • Section 3 “Ordering information” added
02	20030423	-	Product data (9397 750 11279) Modifications: <ul style="list-style-type: none"> • Avalanche ruggedness data added in Table 3 • Correction to Figure 6 • Correction to Figure 11 • Correction to Figure 13
01	20030212	-	Preliminary data (9397 750 11078)

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I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 02 March 2004

Document order number: 9397 750 12756



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